AMENDMENTS TO THE DRAWINGS

The attached annotated sheets of drawings show changes to Figures 1A, 1B, 1C(1), 1C(2) and 3.

The changes to Figure 1A add the reference N4, the bitline references B1, B2, BB2 and BB1 and the node reference N, as shown in the originally filed Figure 1A.

The changes to Figure 1B change the bitline references to BB1, B1, B2, as shown in originally filed Figure 1B.

The changes to Figures 1C(1) and 1C(2) delete all reference characters not explained in the specification, which reference characters are not necessary for an understanding of the invention as Figures 1C(1) and 1C(2) were included in this patent application merely to show relative sizes of the two SRAM cells.

The changes to Figure 3 change "Write" to -- Read --, as shown in originally filed Figure 3, and correct the "Ws" to -- Rs -- to reflect the read (R) operations shown in the top of Figure 3 and explained in the specification.